



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re the Application of: **HASHIMOTO, Hiroshi et al.**

Group Art Unit: **2814**

Serial No.: **09/960,399**

Examiner: **Howard Weiss**

Filed: **September 24, 2001**

**P.T.O. Confirmation No.: 5652**

**FOR: SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION PROCESS  
THEREOF**

**AMENDMENT UNDER 37 CFR §1.111**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Date: November 12, 2004

Sir:

In response to the Office Action dated **July 22, 2004**, please amend the above-identified application as follows:

**Amendments to the Claims** are reflected in the listing of claims which begins on page 2 of this paper.

**Remarks/Arguments** begin on page 18 of this paper.